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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,101	01/29/2004	Chandrasekharan Kothandaraman	2002 P 03440US(10808/138)	9022

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EXAMINER	
WILSON, ALLAN R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/769,101	KOTHANDARAMAN ET AL.	
	Examiner	Art Unit	
	Allan R. Wilson	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because for figures 2A, 3A, and 4A the shading is unclear. Should at least outline each area. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 1 is objected to because of the following informalities: The term "isolated" is confusing. Applicant has not stated in the claim how the gate is isolated (e.g., electrically or physically). Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-3, 10-14 and 16-20 are rejected under 35 U.S.C. 102(e) as being anticipated by 6,617,737 to Hsu et al. (Hsu). Regarding claims 1 and 10, Hsu teaches in figures 2a and b an electrically programmable transistor fuse having a substrate 110 of semiconductor material of a first conductivity type (N-type, col. 3, line 21), a source region 136 and drain region 140

disposed in the substrate and spaced apart to define a channel region (not labeled) therebetween, and a layer of insulating material 122a/124a having a uniform thickness (col. 3, lines 64-67) and disposed over the source region, drain region and channel region, the fuse comprising:

a first gate 124 and a second gate 122 disposed in a single layer of polysilicon (e.g. "single poly" col. 3, line 18) over the insulating material, the first gate disposed overlapping a portion of the source region 136 and the second gate insulated from the first gate (see fig. 2a) and disposed overlapping a portion of the drain region 140 (col. 3, lines 31-35), wherein the first gate includes a terminal for receiving an externally applied signal (word line not shown, col. 3, lines 46-47) and the second gate is capacitively coupled to the drain region (inherent by way of the overlap); and

a coupling device 142 disposed within the substrate and adapted to increase capacitive coupling of the second gate and drain region 140 wherein programming is effectuated by charging the second gate via capacitive coupling with the drain region (col. 4, lines 30-34); and

first circuitry coupled to the first gate terminal (the circuitry of the word line, not shown) and adapted for selecting the transistor fuse for programming via a voltage signal (e.g. –2V as shown in figure 3); and

second circuitry coupled with said drain region 140 and said coupling device and adapted for programming and reading the programming state of the fuse (Hsu teaches in figures 3 and 6 that the device includes circuitry which provides different voltages to the drain and coupling device for programming (fig. 3) and reading (fig. 6)).

Regarding claims 2, 13 and 17, Hsu teaches in figure 3 that programming is effectuated via application of a voltage signal (5V) to the drain region 140 which voltage signal is less than

junction breakdown of the fuse (considered inherent for if the voltage applied were greater than the junction breakdown voltage, the device would cease to operate). Regarding claims 3 and 14, Hsu's drain region 140 may be considered to have an "extended" width as it is formed wider than the source region 136. Regarding claims 11 and 12, it is considered inherent that Hsu's device will include transistors for controlling the programming signal to the drain and coupling device and for detecting current flow therein. Regarding claim 16, Hsu teaches in figure 3 that writing or programming is effectuated by providing a ground voltage (0V) to the source 136, threshold voltage (-2V) to the first gate and programming voltage (5V) to the drain. Regarding claim 18, Hsu teaches in figure 6 and column 5, lines 1-14 a read operation of the device wherein a reference voltage (0V) is applied to the first gate 124 which turns on a channel of the device (col. 5, lines 8-10) and that reading is effectuated by detecting current flow to determine a logic 1 or logic 0 state (col. 1, lines 27-33). That the device be considered "programmed" or "non-programmed" depending on current detection is merely an intended use or function of the device which does not structurally distinguish over Hsu. Regarding claim 19, Hsu teaches that the reference voltage (0V) is greater than the threshold voltage (-2V). Regarding claim 20 as best understood, Hsu teaches that the voltage applied to the first gate during erase (0V) is different from the programming voltage (5V).

Claims 1-10 and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by 5,886,378 to Wang. Regarding claims 1 and 10, Wang teaches in figures 5-7 an electrically programmable transistor fuse having a substrate 134 of semiconductor material of a first conductivity type (P-type, col. 2, line 66), a source region 138 and drain region 140 disposed in

the substrate and spaced apart to define a channel region 144/146 therebetween, and a layer of insulating material 147AB having a uniform thickness (col. 3, lines 4-8) and disposed over the source region, drain region and channel region, the fuse comprising:

a first gate 156 and a second gate 160 disposed in a single layer of polysilicon (col. 3, lines 10-19) over the insulating material, the first gate disposed overlapping a portion of the source region 136 and the second gate insulated from the first gate (see fig. 6) and disposed overlapping a portion of the drain region 140, wherein the first gate includes a terminal for receiving an externally applied signal (not shown, col. 3, lines 43-44) and the second gate is capacitively coupled to the drain region (inherent by way of the overlap); and

a coupling device 142 disposed within the substrate and adapted to increase capacitive coupling of the second gate and drain region 140 wherein programming is effectuated by charging the second gate via capacitive coupling with the drain region (col. 3, lines 32-39); and

first circuitry coupled to the first gate terminal (not shown) and adapted for selecting the transistor fuse for programming via a voltage signal (see again col. 3, lines 43-44, "access transistor must be turned on"); and

second circuitry coupled with said drain region 140 and said coupling device and adapted for programming and reading the programming state of the fuse (see again col. 3, lines 32-39 teaching that the regions 140 and 142 have a high positive voltage applied thereto for programming).

Regarding claim 2, Wang teaches that programming is effectuated by application of a voltage signal to the drain region (col. 3, lines 32-34) and it is considered inherent that the voltage is less than the breakdown voltage of the transistor else the device would cease to

function whereas the device of Wang is designed to be used repeatedly (e.g. programmed and erased). Regarding claims 3, 4, 14 and 15, the limitation "extended width" does not distinguish over Wang since Wang's drain portion may be considered "extended" over a drain region that is more narrowly formed. Also, Wang teaches the device comprising a well region 142 overlapping the second gate 160 (fig. 7) and isolated from the drain 140 (fig. 5). Regarding claims 5-9, 13 and 16-20, these limitations are drawn to the manner in which the device is used; such intended use or functional limitations do not structurally distinguish over Wang and the device of Wang is considered able to perform the cited functions as Wang teaches all the cited structural elements.

Response to Arguments

Applicant's arguments filed 07/26/2005 have been fully considered but they are not persuasive.

The argument that Hsu describes the two gates 122 and 124 are electrically connected by a doped region 132 in the channel is not persuasive. Hsu's floating gate 122 (col. 3, lines 21-23) of transistor 101 is as isolated as Applicants' floating gate 215. Applicants' first and second gates are "serially connected" through the channel.

The argument that Wang describes the two gates 156 and 160 are electrically connected by a doped region 138 in the channel is not persuasive. Wang's gate 160 of transistor 170 is as isolated as Applicants' floating gate 215. Applicants' first and second gates are "serially connected" through the channel.

The argument that "the channel region between the gates includes substrate material" is not persuasive. Hsu clearly illustrates in Fig. 3 the channel region (material from 136 and 140) between the gates 122 and 124 includes substrate material 110. Wang clearly illustrates in Fig. 6 the channel region 144/146 between the gates 156 and 160 includes substrate material 134.

The argument that "neither Hsu nor Wang, disclose a first gate disposed overlapping a. portion of said source region and said second gate isolated from said first gate" is not persuasive. As stated above, Hsu and Wang both disclose a second gate isolated from said first gate. Applicants do not illustrate there is a well in the channel between the gates, but this has not been claimed.

Claims 1-9 and 10-20 stand rejected for the reasons above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allan R. Wilson
Primary Examiner
14 September 2005